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Service Manual

ORDER NO.
CRT4050

CD MECHANISM MODULE(S10.5COMP2-iPod/USB)

CX-3240

This service manual describes the operation of the CD mechanism module incorporated in models listed in the table below.
When performing repairs use this manual together with the specific manual for model under repair.

Model	Service Manual	CD Mechanism Module
DEH-P500UB/XN/UC DEH-P5000UB/XN/UC	CRT4034	CXK5770
DEH-P5050UB/XN/ES DEH-P5050UB/XN/ES1 DEH-P5090UB/XN/ID	CRT4035	CXK5770
DEH-P6000UB/XN/EW5	CRT4036	CXK5770
DEH-P400UB/XS/UC DEH-P4000UB/XS/UC DEH-P4050UB/XS/ES DEH-P4050UB/XU/CN5	CRT4051	CXK5770
DEH-4000UB/XS/EW5 DEH-3050UB/XS/ES DEH-3050UB/XU/CN5	CRT4052	CXK5771
DEH-50UB/XS/EW5	CRT4053	CXK5770
DEH-P4050UB/XN/ES DEH-P4050UB/XN/ES1	CRT4054	CXK 5770

Model	Service Manual	CD Mechanism Module
DEH-5000UB/XS/EW5	CRT4055	CXK5771
DEH-4000UB/X1P/EW5	CRT4056	CXK5771
DEH-3050UB/XN/ES DEH-3050UB/XN/ES1 DEH-3090UB/XN/ID	CRT4059	CXK5771
DEH-P6000UB/X1PEW5	CRT4088	CXK5770
DEH-P5050UB/XU/CN5	CRT4089	CXK5770
DEH-P600UB/XN/UC DEH-P6000UB/XN/UC DEH-P6050UB/XN/ES DEH-P6050UB/XN/ES1	CRT4090	CXK5770
DEH-P7000UB/XN/EW5	CRT4091	CXK5770

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1. CIRCUIT DESCRIPTIONS

The recent mainstay of the CD LSI is the LSI integrating the core DSP with DAC or RF amplifier, which are generally employed as peripheral circuits, however, PE5611B, used in this product, is an LSI integrating the afore-mentioned LSI unit and microcomputer unit in one chip, with an additional USB host control section.

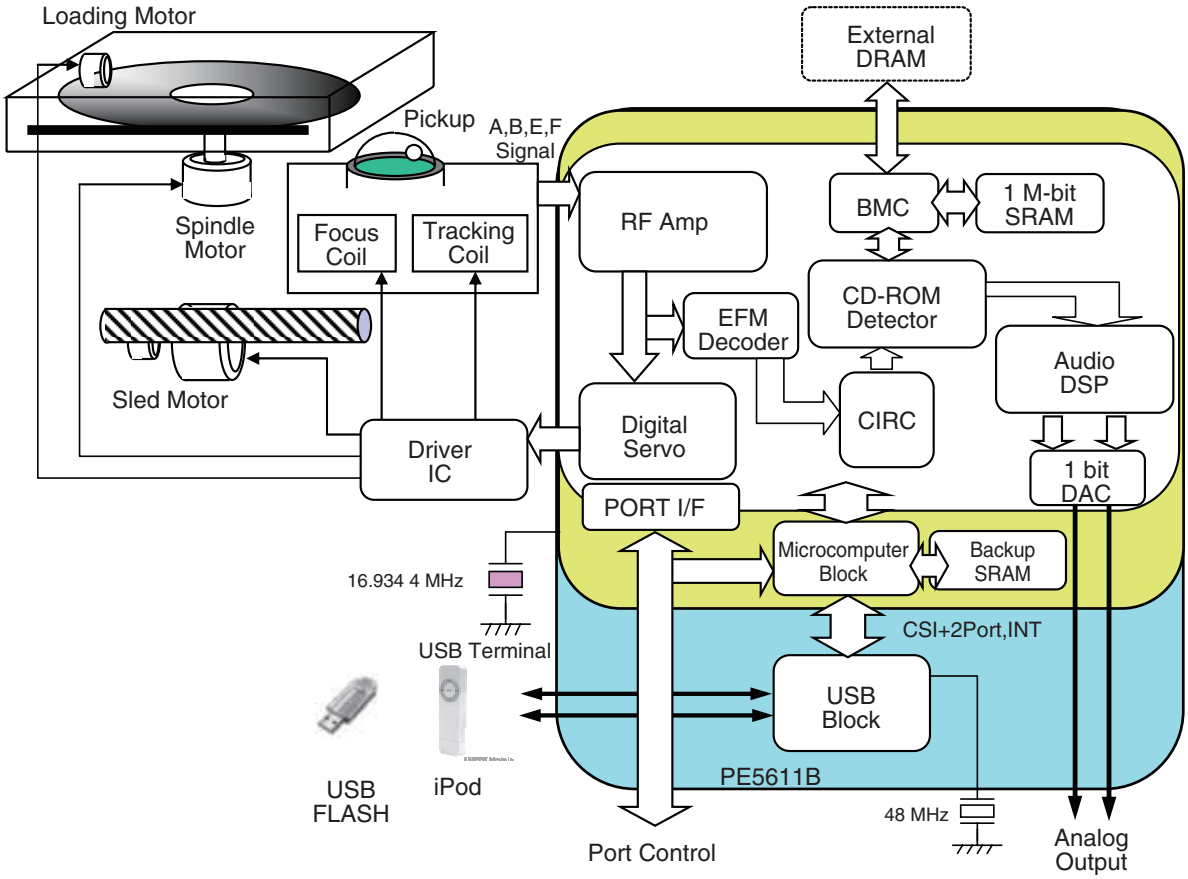


Fig.1.0.1 Block diagram of CD LSI PE5611B

1.1 PREAMPLIFIER BLOCK

In the preamplifier block, the pickup output signals are processed to generate signals that are used in the subsequent blocks: servo, demodulator, and control blocks. Signals from the pickup are I/V converted in the pickup with the preamplifier with built-in photo detectors, and after added with the RF amplifier, they are used to produce such signals as RF, FE, TE, and TE zero-cross signals. The preamplifier block is built in CD LSI PE5611B (IC201), whose parts are described individually below. Incidentally, as this LSI employs a single power supply (+ 3.3 V) specification, the reference voltages of this LSI and the pickup are the REFO (1.65 V) for both. The REFO is an output obtained from REFOUT in the LSI via the buffer amplifier, and is output from the pin 133 of this LSI. All measurements will be performed with this REFO as the reference.

Caution: Be careful not to short-circuit the REFO and GND when measuring.

1.1.1 APC (Automatic Power Control) circuit

Since laser diodes have extremely negative temperature characteristics in optical output when driven in constant current, it is necessary to control the current with the monitor diodes in order to keep the output constant. This is the feature of the APC circuit. The LD current is obtained by measuring the voltage between LD1 and V3R3, and divide the value by 7.5 (ohms), which becomes about 30 mA. The voltage difference between LD and V3R3 will be about 225 mV.

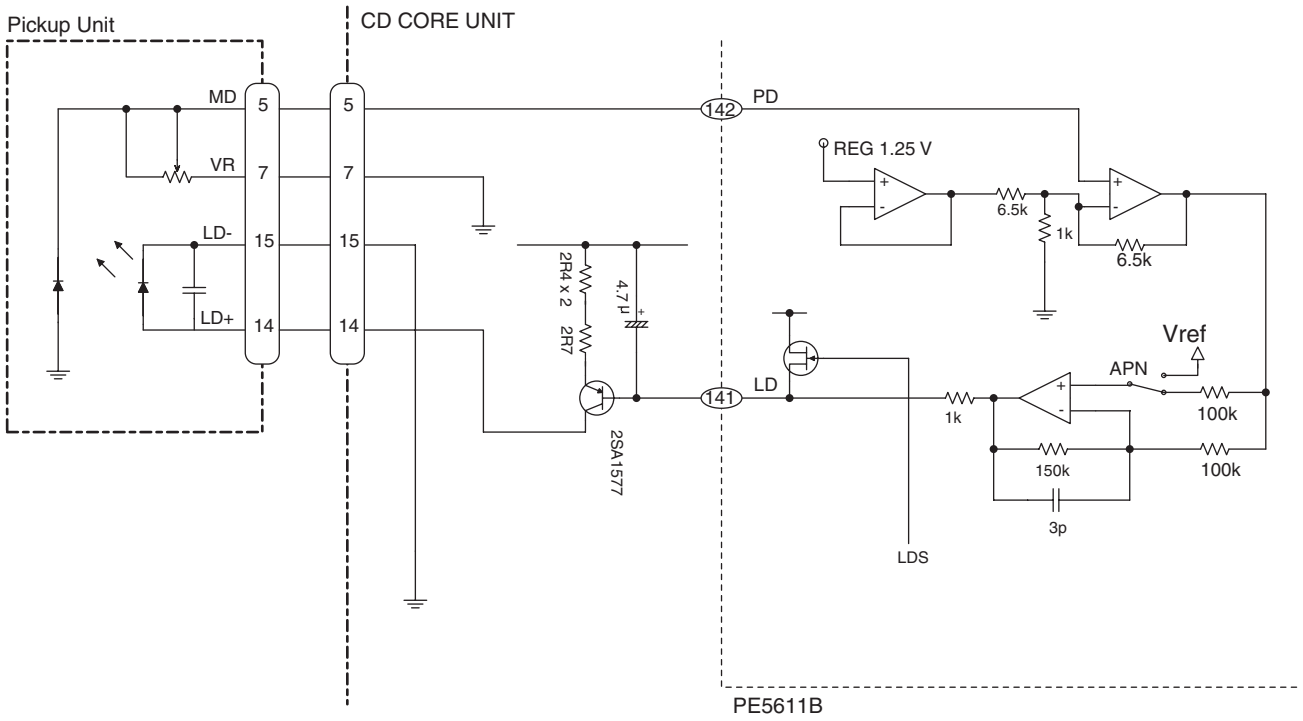


Fig.1.1.1 APC

1.1.2 RF and RFAGC amplifiers

The output from the photo-detector (A + C) and (B + D) is provided from the RFO terminal as the RF signal (which can be used for eye-pattern check), after it is added, amplified, and equalized inside this LSI. The low frequency component of the voltage RFO is calculated as below.

RFO = (A + B + C + D) x 2

The RFO is used for the FOK generation circuit and RF offset adjustment circuit.

The RFO signal, output from the pin 122, is A/C-coupled externally, input to the pin 121, and amplified in the RFAGC amplifier to obtain the RFAGC signal.

Also, this LSI is equipped with the RFAGC auto-adjustment function, explained below, which switches feedback gains of the RFAGC amplifier so that the RFO output will be 1.5 V.

This RFO signal is also used for the EFM, DFCT, MIRR, and RFAGC auto-adjustment circuits.

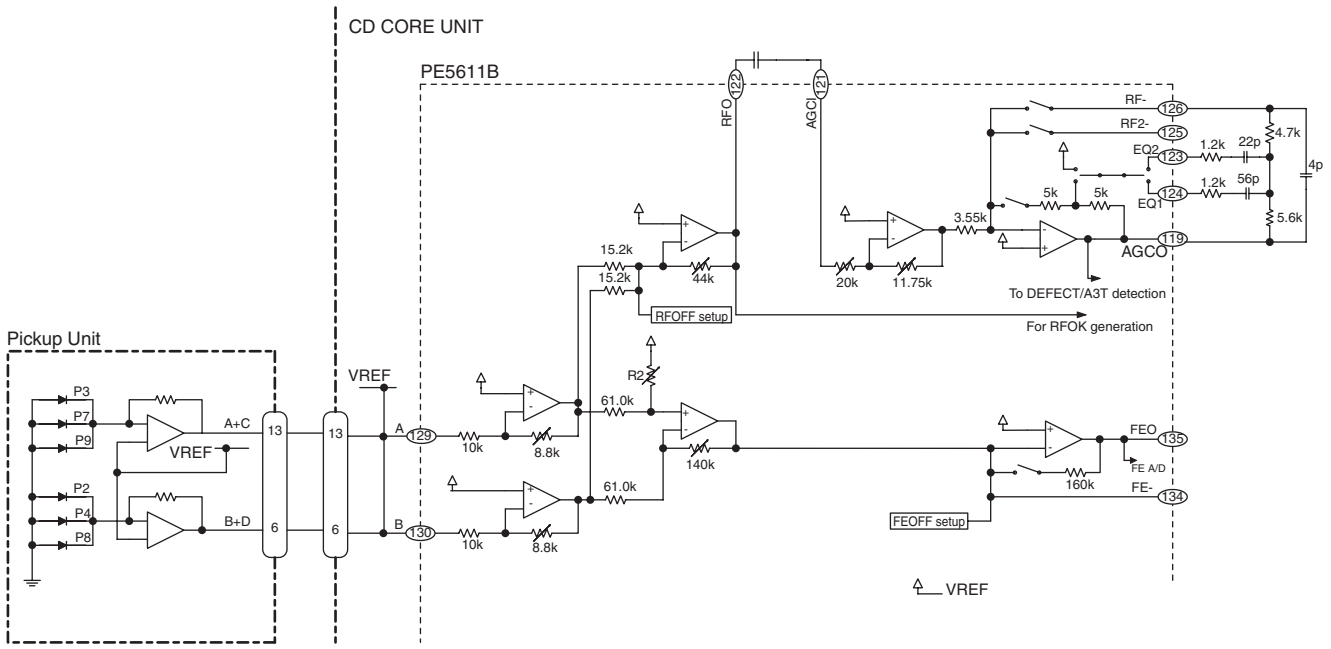


Fig.1.1.2 RF/AGC/FE

1.1.3 Focus error amplifier

The photo-detector outputs (A + C) and (B + D) are passed through the differential amplifier and the error amplifier, and (A + C - B - D) is provided from the pin 135 as the FE signal. The low frequency component of the voltage FE is calculated as below.

FE = (A + C - B - D) x 8.8k / 10k x 111k / 61k x 160k / 72k

= (A + C - B - D) x 3.5

For the FE outputs, an S-shaped curve of 1.5 Vp-p is obtained with the REFO as the reference. The cutoff frequency for the subsequent stage amplifiers is 14.6 kHz.

1.1.4 RFOK circuit

This circuit generates the RFOK signal, which indicates the timing to close the focus loop and focus-close status during the play mode, from the pin 70. As for the signal, "H" is output in closing the focus loop and during the play mode.

Additionally, the RFOK becomes "H" even in a non-pit area, since the DC level of the RFO signal is peak-held in the subsequent digital block and compared at a certain threshold level to generate the RFOK signal. Therefore, the focus is closed even on a mirror-surface area of a disc. This signal is also supplied to the microcomputer via the low-pass filer as the FOK signal, which is used for protection and gain switching of the RF amplifier.

1.1.5 Tracking error amplifier

The photo-detector outputs E and F are passed through the differential amplifier and the error amplifier to obtain (E - F), and then provided from the pin 138 as the TE signal. The low frequency component of the voltage TE is calculated as below.

TEO = (E - F) x 63k / 112k x 160k / 160k x 181k / 45.4k x 160k / 80k

= (E - F) x 4.48

For the TE output, TE waveform of about 1.3 Vp-p with the REFO as the reference. The cutoff frequency in the subsequent is 21.1 kHz.

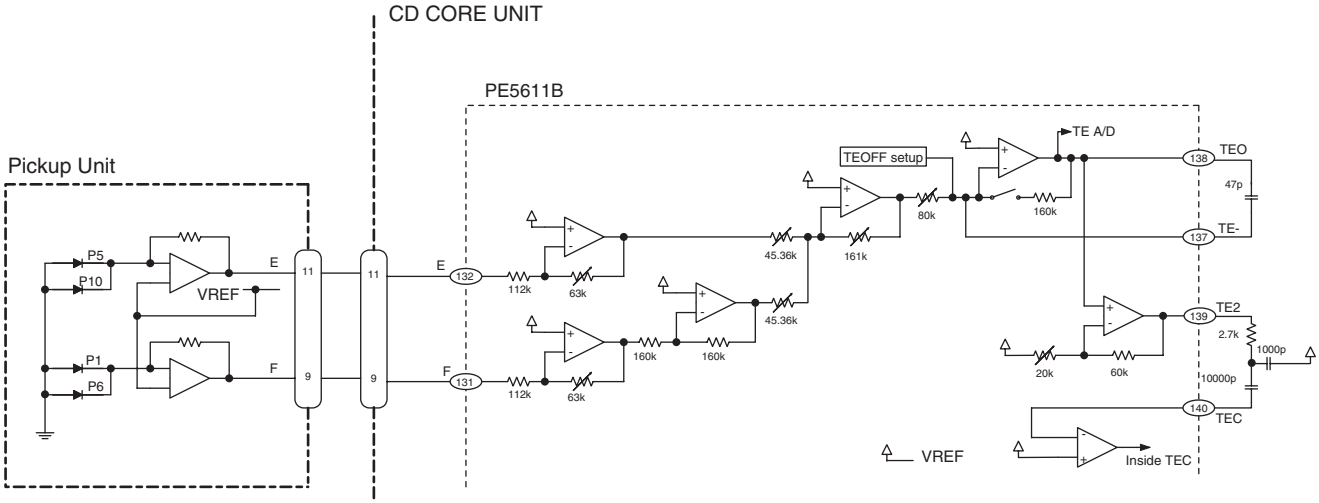


Fig.1.1.3 TE

1.1.6 Tracking zero-cross amplifier

The tracking zero-cross signal (hereinafter referred to as TEC signal) is obtained by amplifying the TE signal by fourfold, and used to detect the tracking-error zero-cross point. As the purpose of detecting the zero-cross point, the following two points can be named:

1. To use for track-counting in the carriage move and track jump modes
2. To use for detecting the direction in which the lens moves in tracking close. (Used in the tracking brake circuit to be explained later.)

The frequency range of the TEC signal is from 300 Hz to 20 kHz, and

TEC voltage = TE level x 4

The TEC level can be calculated at 4.62 V, which, at this level, exceeds the D range of the operational amplifier, and clips the signal, but, because the CD LSI only uses the signal at the zero-cross point, it poses no particular problem.

1.1.7 EFM circuit

The EFM circuit converts the RF signal into digital signals of 0 and 1. The AGCO signal output from the pin 119 is A/C-coupled externally, input to the pin 118, and supplied to the EFM circuit.

Missing RF signal due to scratches and stains on the disc, and asymmetry of the upper and lower parts of the RF, caused by variation in disc production, cannot be entirely eliminated in AC coupling process, the reference voltage ASY of the EFM comparator is controlled, using the probability that 0 and 1 occur at 50%. Thus, the comparator level will always stay around the center of the RFO signal. This reference voltage ASY is generated by passing the EFM comparator output through the low-pass filter. The EFM signal is output from the pin 113.

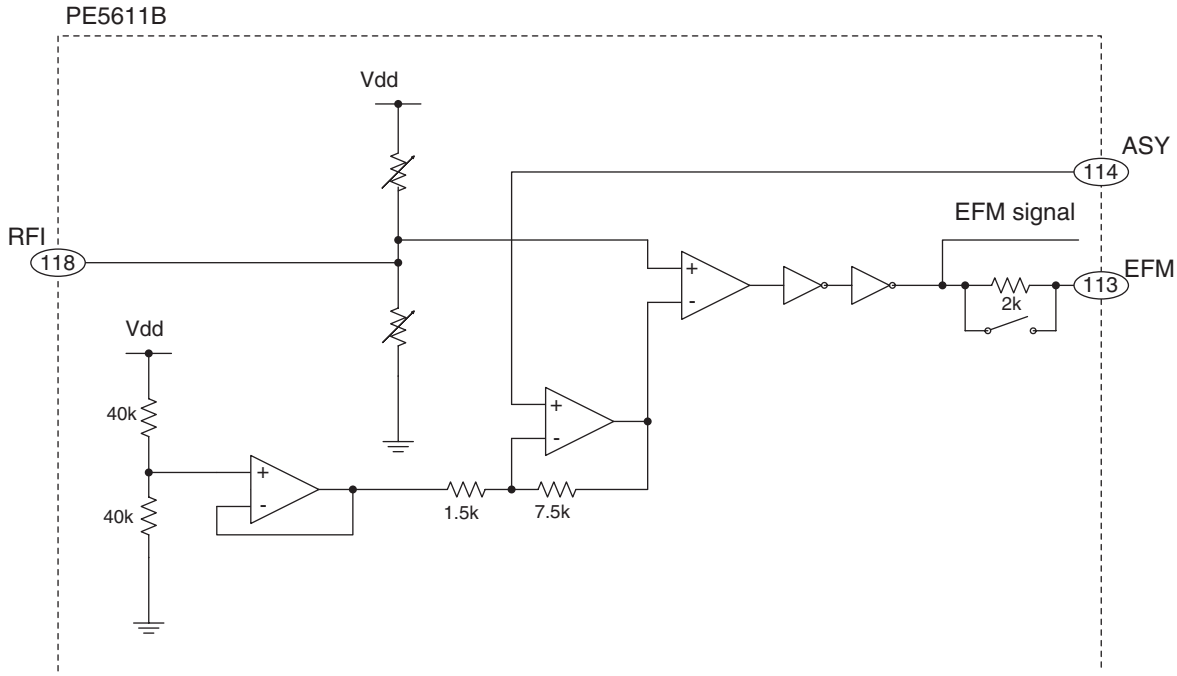


Fig.1.1.4 EFM

1.2 SERVO BLOCK (PE5611B: IC201)

The servo block performs servo control such as error signal equalizing, in-focus, track jump and carriage move. The DSP block is the signal-processing unit, where data decoding, error correction, and compensation are performed. The FE and TE signals, generated in the preamplifier stage, are A/D-converted, and output drive signals for the focus, tracking, and carriage systems via the servo block. Also, the EFM signal is decoded in the signal-processing unit, and ends up in outputting D/A-converted audio signals through the D/A converter. Furthermore, in this decoding process, the spindle servo error signal is generated, supplied to the spindle servo block, and used to output the spindle drive signal.

Each drive signal for focus, tracking, carriage, and spindle servos (FD, TD, SD, and MD) are output as PWM3 data, and then converted to analog data through the LPF. These drive signals, after changed to analog form, can be monitored with the FIN, TIN, CIN, and SIN signals, respectively. Subsequently, the signals are amplified and supplied to the actuator and motor for each signal.

1.2.1 Focus servo system

The main equalizer of the focus servo consists of the digital equalizer block. The figure 1.2.1 shows the block diagram of the focus servo system.

In the focus servo system, it is necessary to move the lens within the in-focus range in order to close the focus loop. For that purpose, the in-focus point is looked for by moving the lens up and down with the focus search voltage of triangular signal. During this time, the rotation of the spindle motor is retained at a certain set speed by kicking the spindle motor.

The servo LSI monitors the FE and RFOK signals and automatically performs the focus-close operations at an appropriate timing. The focus-close operation is performed when the following three conditions are satisfied at the same time:

1) The lens moves toward the disc surface.

2) RFOK = "H"

3) The FE signal is zero-crossed.

Consequently, the FE converges to "0" (= REFO).

When the above-mentioned conditions are met and the focus loop is closed, the FSS bit is shifted from "H" to "L," and then, in 10 ms, the CPU of the LSI starts monitoring the RFOK signal obtained through the low-pass filter.

If the RFOK signal is determined to be "L," the CPU of the LSI takes several actions including protection.

Fig.1.2.2 shows a series of actions concerning the focus close operations. (It shows a case where the focus loop cannot be closed.)

With the focus mode selector displaying 01 in the test mode, pressing the focus close button, allows to check the S-shaped curve, search voltage, and actual lens behavior.

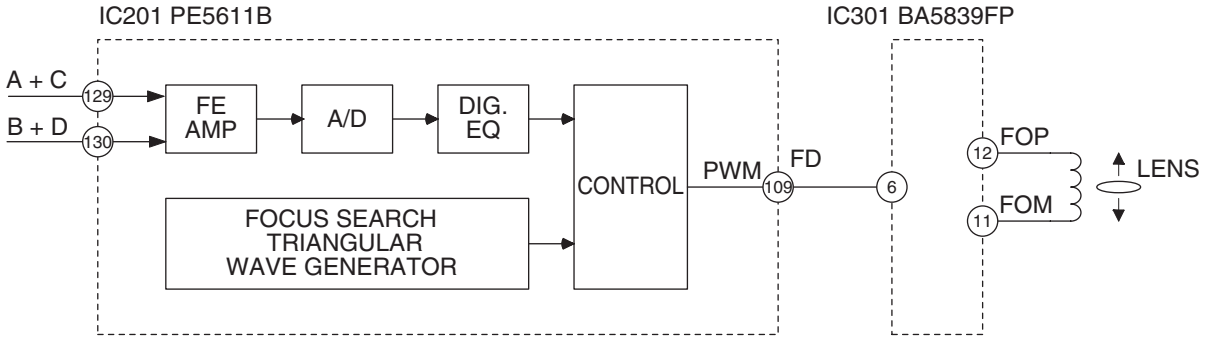


Fig.1.2.1 Block diagram of the focus servo system

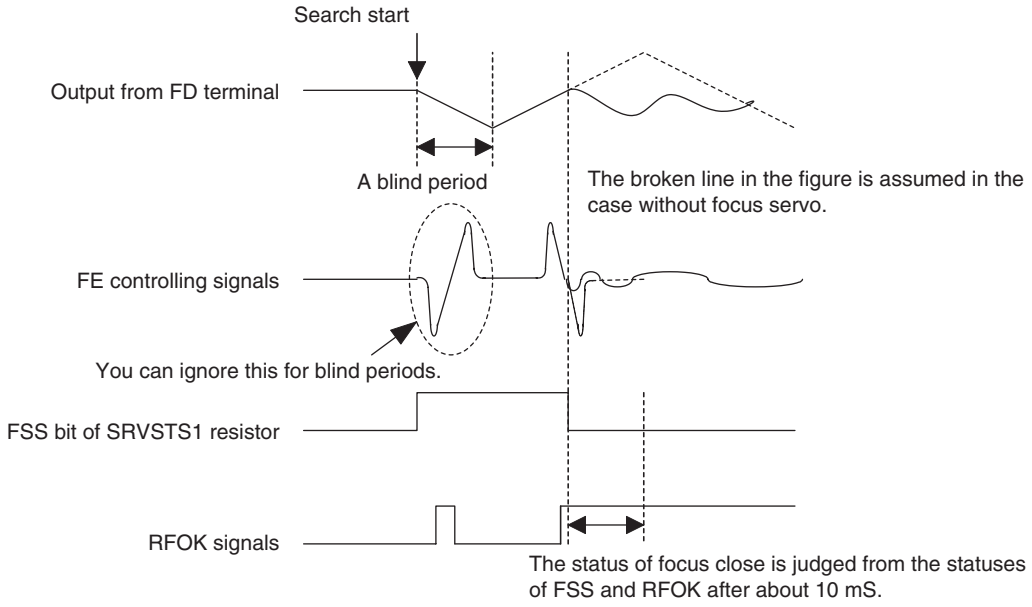


Fig.1.2.2 Timing chart for focus close operations

1.2.2 Tracking servo system

The main equalizer of the tracking servo consists of the digital equalizer block. The figure 1.2.3 shows the block diagram of the tracking servo system.

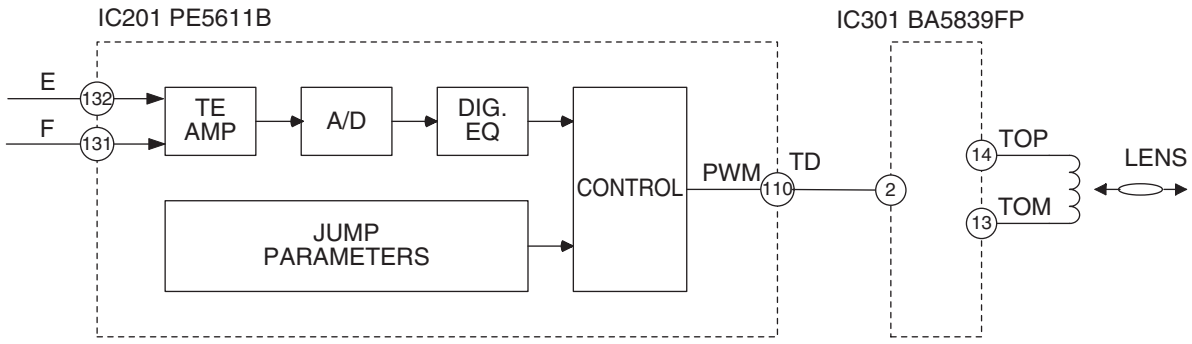


Fig.1.2.3 Block diagram of the tracking servo system

(a) The track jump operation is automatically performed by the auto-sequence function inside the LSI with a command from the CPU of the LSI. For the track jumps used in the search mode, a single track jump and four to 100 multi-track jump are available in this system. In the test mode, out of these track jumps, 1, 32, and 32 * 3 track jumps, as well as carriage move can be performed and checked in mode selection. In a track jump, the CPU of the LSI sets about half the number of the total tracks to jump (about five tracks for a 10-track jump), and the set number of tracks are counted using the TEC signal. By outputting the brake pulse for a certain period of time (set by the CPU of the LSI) from the time the set number is counted, and stopping the lens, the tracking loop can be closed so that the normal play can be continued.

Also, in order to facilitate closing of the tracking loop in a track jump, the brake circuit is kept ON for 50 msec, after the brake pulse is stopped, for increasing the tracking servo gain. The FF/REW action in the normal operation mode is realized by performing single jumps consecutively. The speed is approximately 10 times faster than in the normal mode.

(b) Brake circuit

Since the servo loop is not closed very well in the setup mode and track jump mode, the brake circuit is used for stabilizing the servo-loop close operation. The brake circuit detects the direction in which the lens moves, and outputs only the drive signal for the direction opposite to the movement to slow down the lens, thereby stabilizing the tracking servo-loop close operation. Additionally, the off-track direction is determined from the TEC and MIRR signals, as well as their phase relation.

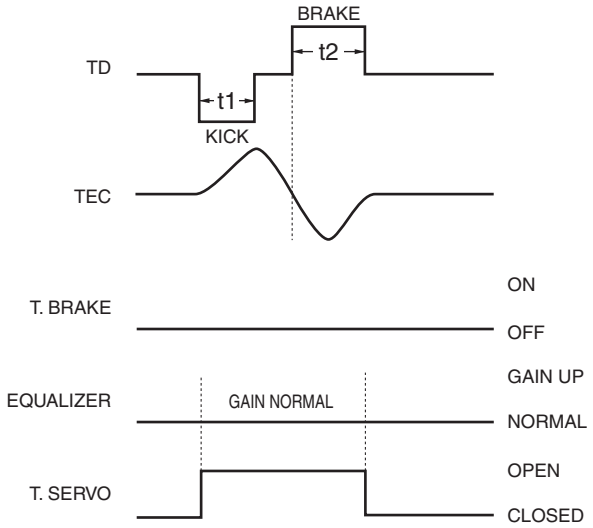


Fig.1.2.4 Single-track jump

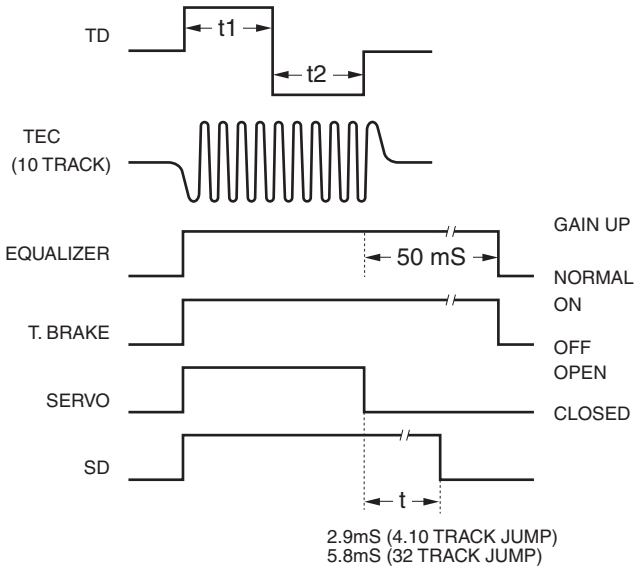
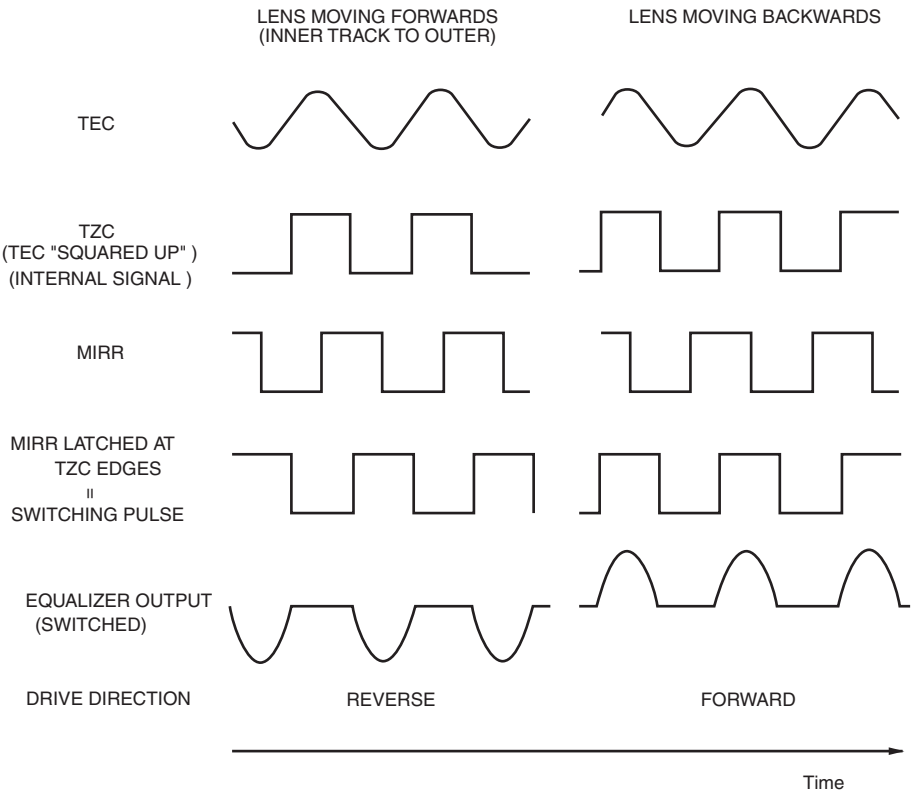


Fig.1.2.5 Multi-track jump



Note : Equalizer output assumed to hava same phase as TEC.

Fig.1.2.6 Track brake

1.2.3 Carriage servo system

The carriage servo system inputs the output of the low frequency component from the tracking equalizer (information on the lens position) to the carriage equalizer, and, after the gain is increased to a certain level, outputs the drive signal from the CD of the LSI. This signal is applied to the carriage motor via the driver IC.

Specifically, since it is necessary to move the whole pickup to the FORWARD direction when the lens offset reaches a certain level during the play mode, the equalizer gain is set to output higher voltage than the carriage motor starting voltage at this time. In actual operations, a certain threshold level is preset in the servo LSI for the equalizer output, and only when it exceeds the threshold level, the drive voltage will be output. This can reduce the power consumption. Also, before the whole pickup starts moving, the equalizer output voltage may exceed the threshold level a few times, due to such causes as eccentricity of discs. In this case, the output waveform of the drive voltage from the LSI assumes a pulse-like form.

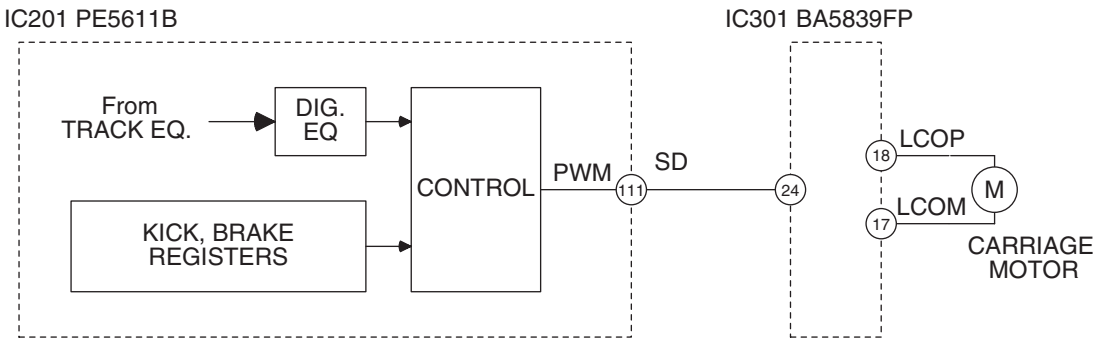


Fig.1.2.7 Block diagram for the carriage servo block

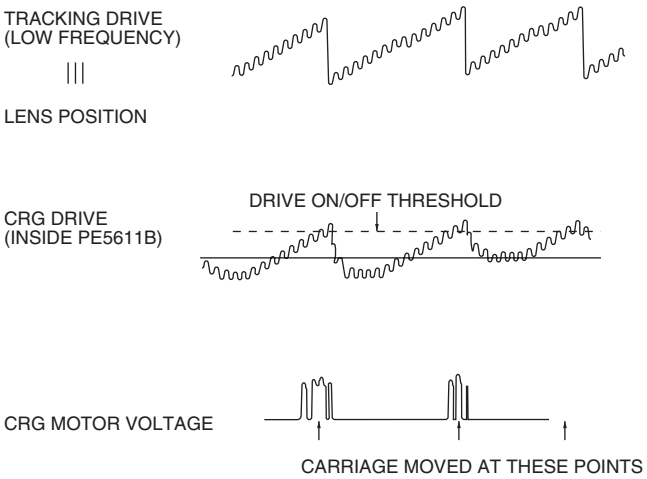


Fig.1.2.8 Waveforms of the carriage signal

1.2.4 Spindle servo system

In the spindle servo system, the following modes are available:

1) Kick

Used to accelerate the disc rotation in the setup mode.

2) Offset

a. Used in the setup mode after the kick mode, until the TBAL adjustment is completed.

b. Used during the play mode when the focus loop is unlocked, until it is locked again.

In both cases, the mode is used to keep the disc rotation approximately normal.

3) Applicable servo

CLV servo mode, used in the normal operation.

In the EFM demodulation block, by WFCK/16 sampling whether the frame sync signal and the internal frame counter output are synchronized, a signal is created to show if they are "in-sync" or "non-sync." The status is not recognized as asynchronous until the signal is "non-sync" for eight consecutive times; otherwise it is recognized as synchronous. In the applicable servo mode, the leading-in servo mode is automatically selected in the asynchronous status, and the normal servo mode in the synchronous status.

4) Brake

Used to stop the spindle motor.

In accordance with the CPU of the LSI command, the brake voltage is sent out from the servo LSI. At this time, the EFM waveform is monitored inside the CD of the LSI, and when the longest EFM pattern exceeds a certain interval (or the rotation slows down enough), a flag is set inside the CD of the LSI, and the CPU of the LSI switches off the brake voltage. If a flag is not set within a certain period, the CPU of the LSI shifts the mode from the brake mode to the stop mode, and retains the mode for a certain period of time. If the mode switches to this stop mode in the eject operation, the disc will be ejected after the period of time mentioned above elapses.

5) Stop

Used when the power is turned on and during the eject operation. In the stop mode, the voltage in both ends of the spindle motor is 0 V.

6) Rough servo

Used in carriage feed (carriage move mode such as long search).

By obtaining the linear velocity from the EFM waveform, the "H" or "L" level is input to the spindle equalizer. In the test mode, this mode is also used for grating confirmation.

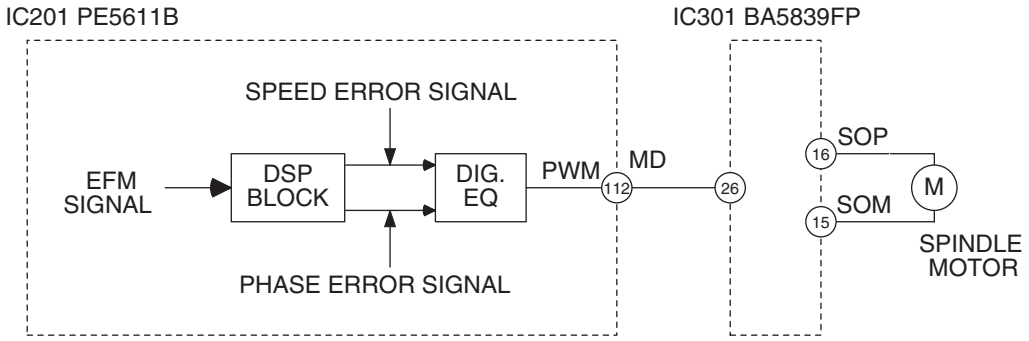


Fig.1.2.9 Block diagram of the spindle servo system

1.3 AUTOMATIC ADJUSTMENT FUNCTION

In this system, all the circuit adjustments are automated inside the CD of the LSI.
All adjustments are performed whenever a disc is inserted or the CD mode is selected by pressing the source key.
Details of each adjustment will be explained below.

1.3.1 TE, FE, and RF offset auto-adjustment

In this adjustment the TE, FE, and RF amplifier offsets of the preamplifier block in POWER ON are adjusted to the respective target values with the REFO as reference. (The target values for TE, FE, and RF offsets are 0 V, 0 V, and - 0.8 V, respectively.)

Adjusting procedure

1) The CPU of the LSI reads respective offsets through the CD of the LSI, when they are in LDOFF status.
2) The CPU of the LSI calculates the voltages for correction from the values read in 1), and substitutes the corrected values to prescribed places to adjust.

1.3.2 Tracking balance (T.BAL) auto-adjustment

This adjustment equalizes the output difference of the E-ch and F-ch from the pickup by changing the amplifier gain inside the CD of the LSI. In actual operation, adjustment is performed so that the TE waveform becomes symmetrical on each side of the REFO.

Adjusting procedure

1) After closing the focus loop,
2) Kick the lens in the radial direction to ensure the generation of the TE waveform.
3) The CPU of the LSI reads the offset amount of the TE signal calculated in the LSI at the time through the CD of the LSI.
4) The CPU of the LSI determines the offset amount is 0, positive, or negative.
- When the offset amount is 0, the adjustment is completed.
- When the offset amount is positive or negative, the amp gains for E-ch and F-ch should be changed, following a certain rule.

Then, steps 2) to 4) are repeated until the offset amount becomes 0 or the repetition reaches the limit number of times.

1.3.3 FE bias auto-adjustment

This adjustment is to maximizes the RFO level by optimizing the focus point during the play mode, utilizing the phase difference between the 3T level waveform of the RF waveform and that of when focus error disturbance is input. This adjustment is performed at the same timing as the auto-gain control, which will be described later, since disturbance is input to the focus loop.

Adjusting procedure

1) The CPU of the LSI issues the command to introduce disturbance to the focus loop (inside the CD of the servo LSI).
2) The waver of the 3T component of the RF signal is detected in the CD of the LSI.
3) The relation between the 3T component above and the disturbance is processed inside the CD of the LSI to detect the volume and direction of the focus offset.
4) The CPU of the LSI issues a command and reads out the detected results from the CD of the LSI.
5) The CPU of the LSI calculates the necessary correction and substitutes the result to the bias adjustment term inside the CD of the LSI.

Additionally, in this adjusting, a series of steps are repeated for better adjustment accuracy, the same as in the auto-gain control.

1.3.4 Focus and tracking AGC

This adjustment is to automatically adjust the focus and tracking servo loop gains.

Adjusting procedure

1) Introduce disturbance to the servo loop.

2) The error signals (FE and TE) when disturbance is introduced are extracted through the band pass filter, to obtain the G1 and G2 signals.

3) The CPU of the LSI reads the G1 and G2 signals through the CD of the LSI.

4) The CPU of the LSI calculates the necessary correction and performs the loop gain adjustment inside the CD of the LSI.

For increased adjustment accuracy, the same adjustment process is repeated a few times.

1.3.5 RF level auto-adjustment (RFAGC)

This adjustment is to adjust the dispersion of the RF level (RFO), which may be caused by mechanism or disc-related factors, to a steady value for reliable signal transmission. The adjustment is performed by changing the amp gain between RFO and RFAGC.

Adjusting procedure

1) The CPU of the LSI issues a command and reads out the output from the RF level detection circuit inside the CD of the LSI.

2) From the read values, the CPU of the LSI calculates the amp gain to change the RFO level to the target.

3) The CPU of the LSI sends a command to the CD of the LSI to adjust the amp gain to the level calculated in 2).

This adjustment is performed

1) when only the focus close operation is completed during the setup mode, and

2) immediately before the setup is completed (or when the play mode is about to start).

1.3.6 Adjustment of gains in preamplifier stage

In this adjustment, when reflected beams from the disc surface are extremely weak, such as when the lens is dirty, or a CD-RW is played, gains in the whole RFAMP block (FE, TE, and RF amplifiers) are increased by + 6 dB or + 12 dB, depending on the situation.

Adjusting procedure

When the system determines that the reflected beams from the disc surface are extremely weak during the setup mode, the whole RFAMP gains will be increased by + 6 dB or + 12 dB.

1.3.7 Initial values in adjustment

All automatic adjustments immediately after inserting a disc are performed based on the initial values. Automatic adjustments by source change or ACC ON are basically performed using the previous adjustment values as the initial values.

1.3.8 Coefficient display of adjustment results

For some of the adjustments (FE and RF offset, FZD cancel, F and T gains, and RFAGC), the adjustment results can be displayed and confirmed in the test mode.

The coefficient display in each auto adjustment is as follows:

1) FE and RF offset

Reference value = 32 (coefficient of 32 indicates that no adjustment is required)

The value is displayed in the unit of approximately 32 mV.

Ex. When the FE offset coefficient is 35,

35 - 32 = 3 x 32 mV = 96 mV

The correction is about +96 mV, which means the FE offset before adjustment is - 96 mV.

2) F and T gain adjustment

Reference value for focus and tracking = 20

The displayed coefficient / the reference value indicates the adjusted gain.

Ex. When the AGC coefficient is 40,

adjustment of 40 / 20 = 2 times (+ 6 dB) has been performed.

(It means that the original loop gain was half the target, and the whole gain was doubled to obtain the target value.)

3) RF level adjustment (RFAGC)

Reference value = 8

The coefficient of 9 to 15 indicates to increase the RF level

(for more gains).

The coefficient of 7 to 10 indicates to decrease the RF level

(for less gains).

When the coefficient changes by 1, the gain changes by 0.7 to 1 dB.

When the coefficient is 15, the gain is the maximum at TYP + 7.9 dB.

When the coefficient is 0, the gain is the minimum at TYP - 4.6 dB.

1.4 POWER SUPPLY AND LOADING BLOCK

For the power supply for this system, the VD (7.5 ± 0.5 V) and the VDD (3.3 ± 0.165 V), which are supplied from the motherboard, are used. The two power supplies, the VD mentioned above (for the drive system), and the VDD (for the LSI: 3.3 V), are used in this system.

The CPU of the LSI controls ON/OFF with "CONT", except for Load/Eject of the CD driver. For ON/OFF of the Loading drive, no particular control terminals are available, but the input signal "LOEJ" assumes an equivalent role. Also, the LCO output switches LOADING MODE and CARRIAGE MODE with "CLCONT".

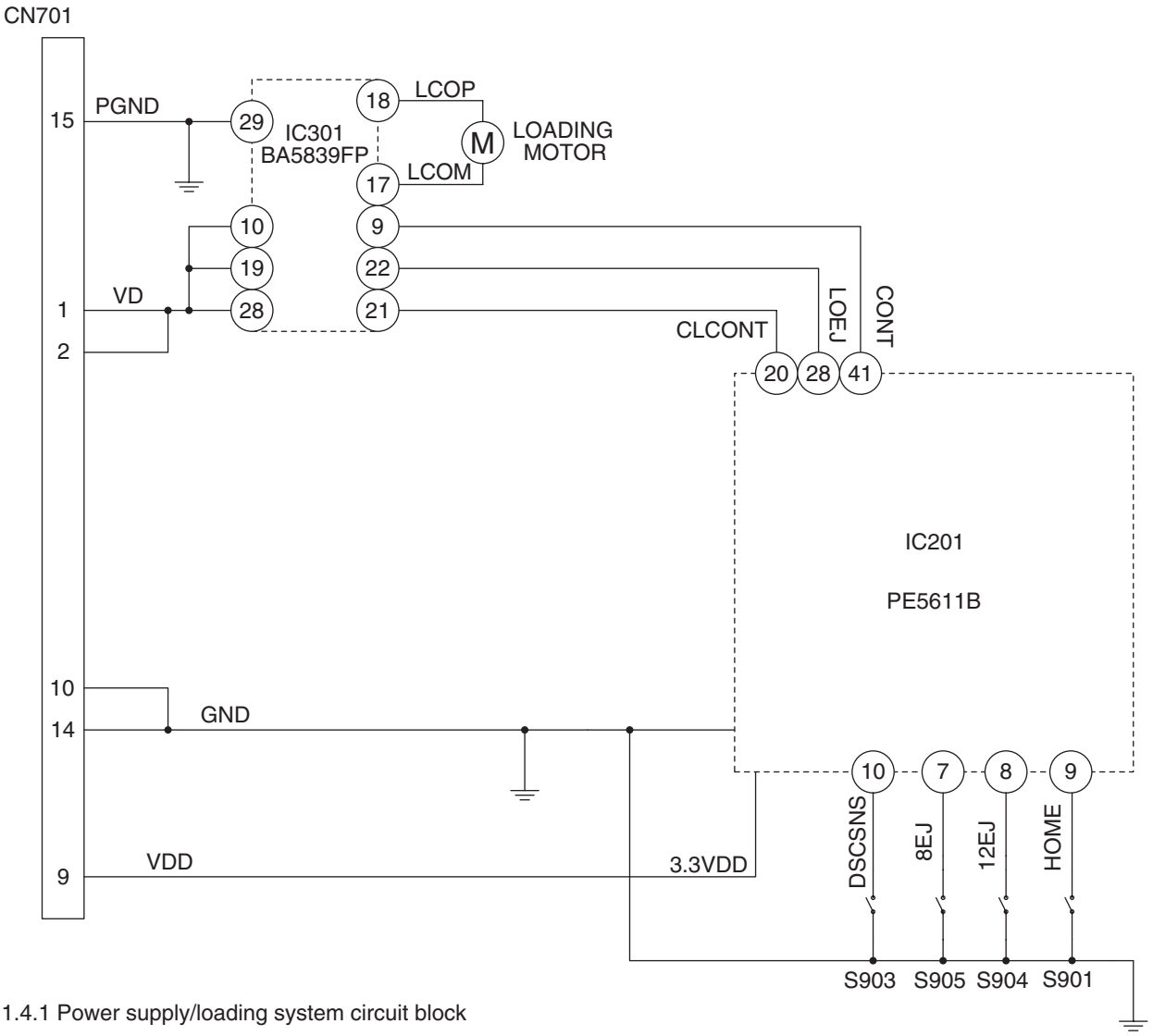


Fig.1.4.1 Power supply/loading system circuit block

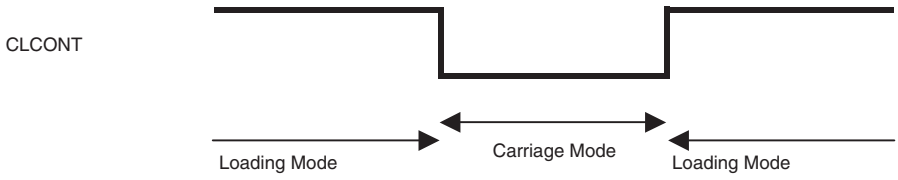


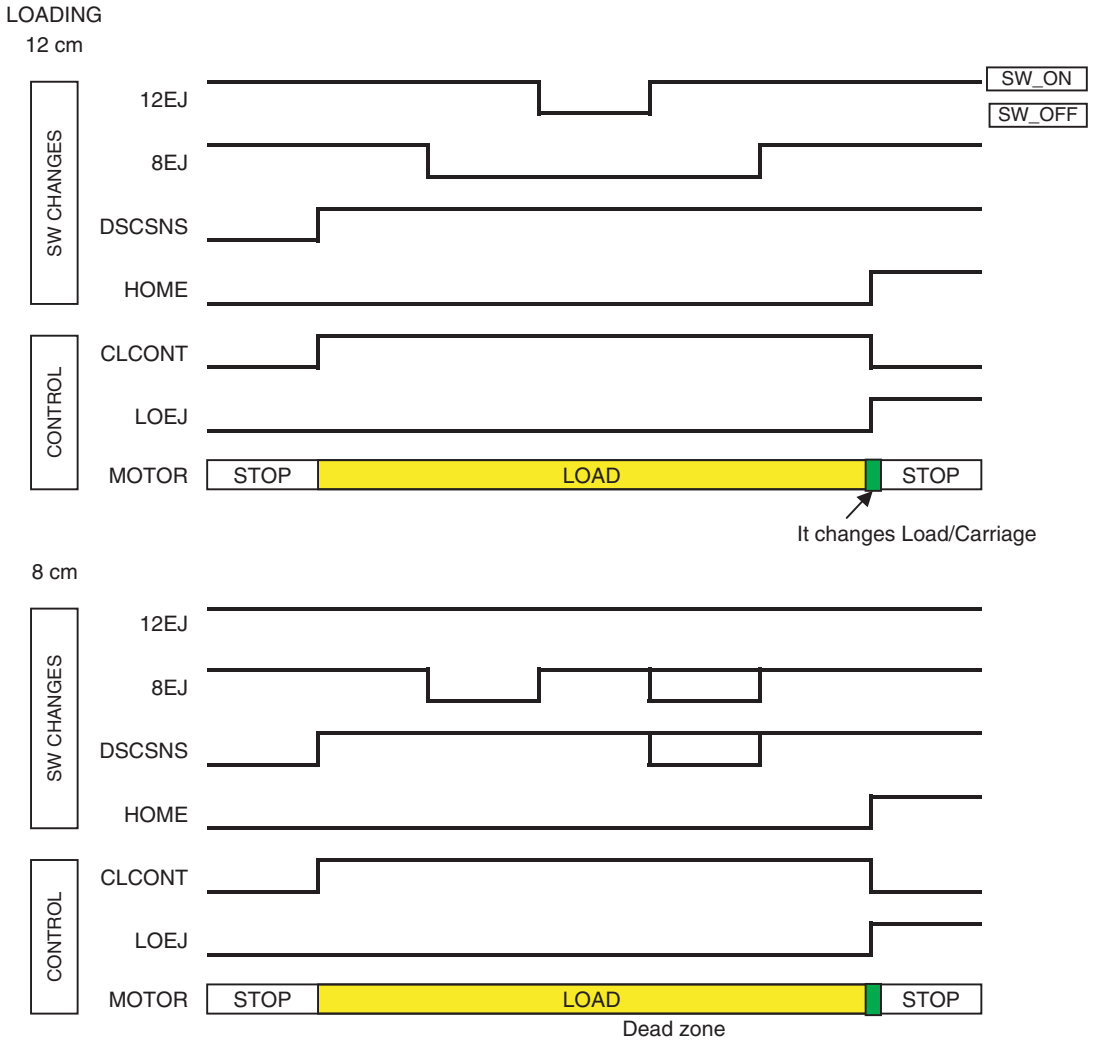
Fig.1.4.2 Loading/carriage mode shift

The load/eject operation is controlled with the status changes of the HOME switch (also used for clamp detection) on the mechanism unit and the three switches on the control unit. The ON/OFF statuses of these switches are respectively detected at the input port of the microcomputer.

Using the detection results in the microcomputer, each status (A to E) is determined. The disc size detection (8 or 12 cm) is also performed through this status change. Each status is shown in Fig.1.4.3 and the status change in Fig.1.4.4.

	Status	A	B	C	D	E
DSCSNS	SW1(S903)	OFF	ON	ON	ON	ON
8SW	SW2(S905)	ON	ON	OFF	OFF	ON
12SW	SW3(S904)	ON	ON	ON	OFF	ON
HOME	SW4(S901)	OFF	OFF	OFF	OFF	ON
	Mechanism state	With no disc	-	-	-	Clamp state

Fig.1.4.3 DSCSNS status



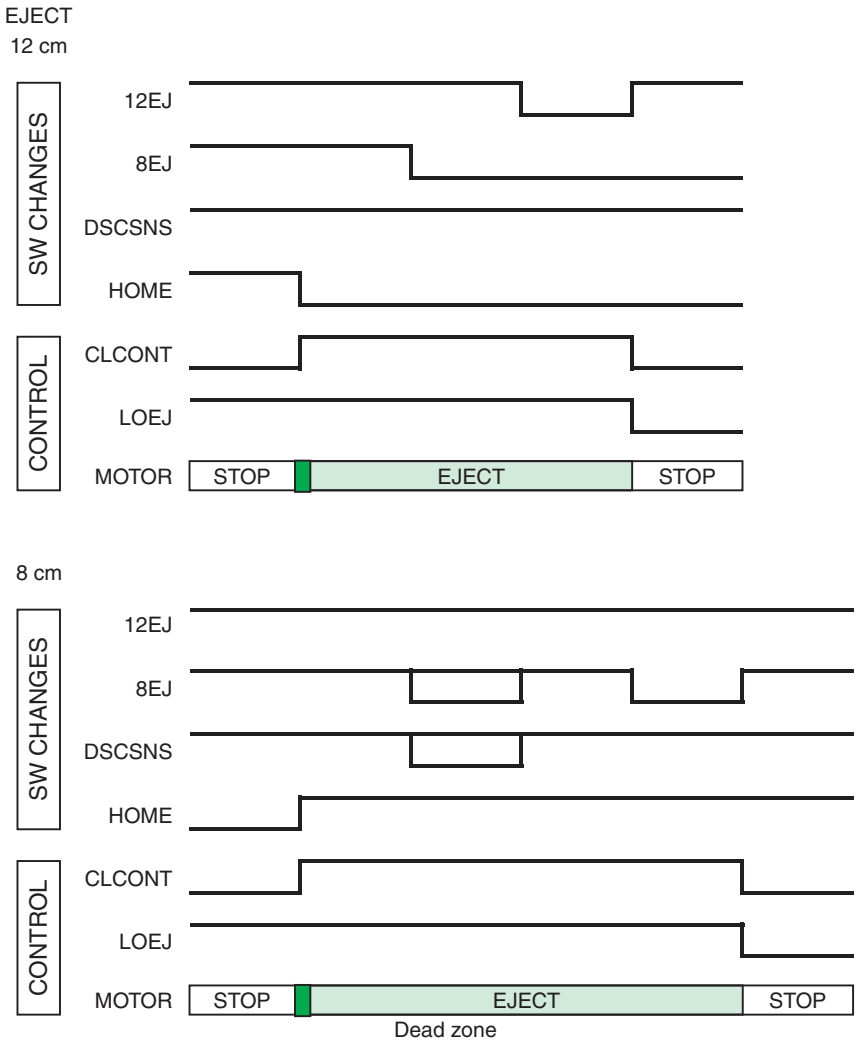


Fig.1.4.4 Status change in LOAD and EJECT modes

1.5 USB BLOCK

1.5.1 Outline

This product has a built-in USB2.0FS host controller and reads the compressed audio data from USB memory, portable device (MSC) or iPod.
The read data is transmitted to the LSI CPU block via the bus bridge connected to the USB host and serial interface and then to the LSI CD block.

1.5.2 Block diagram of USB functions

The USB host controller implements control from the PCI bridge in bus bridge via the PCI bus.
Compressed audio data of Mass Storage class is loaded into the bus bridge in Bulk transfer from USB device using DP (USB data +) and DM (USB data -).
The bus bridge controls by microcontroller serial transfer, universal port and external interrupt.
Compressed audio data received in serial transfer is transferred to the audio DSP in LSI CD block via the LSI CPU block and is reproduced.

The functions of the USB host controller and bus bridge are described as follows:

[USB host controller]

- Loads the compressed audio data from the USB device connected to the USB connector.
- OpenHCI Specification Release 1.0a compliant
- Supports Full-Speed (12 Mbps) USB devices.
- Supports Mass Storage class and Bulk transfer.
- System clock: 48 MHz (with clock oscillation stopping function)
- PCI clock: pclk = 27 MHz

[Bus bridge]

- Bridge circuit to connect between the USB host controller and LSI CPU block
- Decodes the serial data and converts it for PCI bus.
- Converts the data from PCI bus to serial data.
- Transfers directly to the RAM in USB_HOST bridge.
- PCI clock: pclk = 27 MHz
- Serial clock: sclk = 8.467 MHz

The block diagram of USB functions are provided as follows:

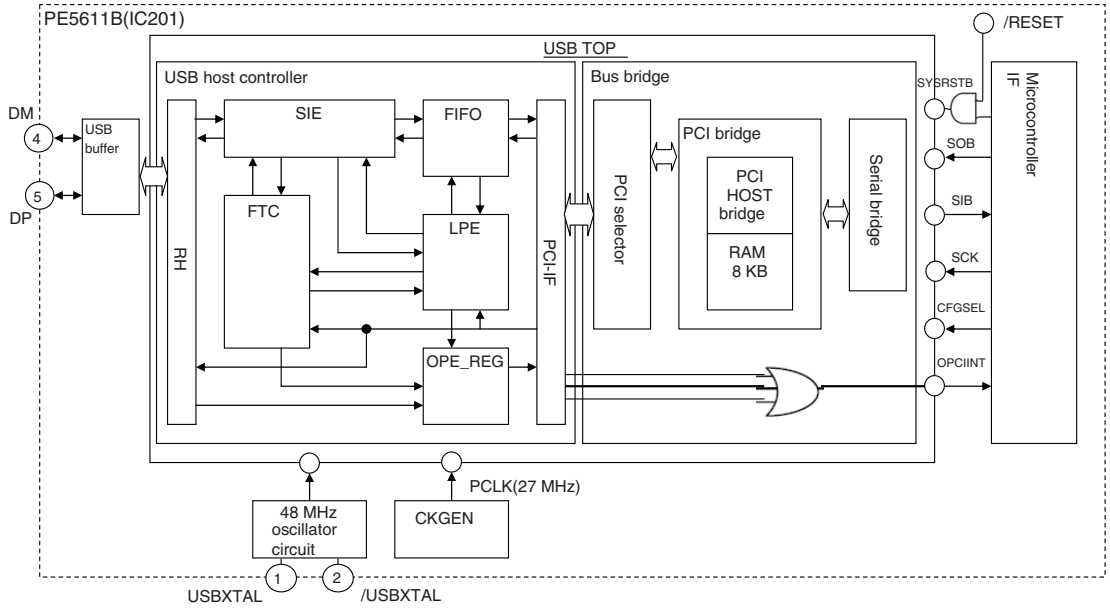


Fig.1.5.1 Block diagram of USB functions

[Description of block diagram of USB functions]
<USB host controller>

PCI_IF: Module for communication between the internal circuits of Host and PCI bus
FIFO: FIFO module for asynchronism absorption between the USB clock and PCI clock
LPE: Module to implement USB list processing
SIE: Module to implement serial-parallel and parallel-serial conversion, CRC processing and bit stuffing process on USB transfer data
FTC: Module to implement frame control for USB
RH: Module with the role of RootHub for USB. Implements USB buffer control.

<Bus bridge>

A circuit to connect between the serial I/F of LSI CPU block and USB host controller
Serial bridge: Module to connect between the microcontroller and PCI HOST bridge
PCI HOST bridge: Module to connect between the PCI bus, memory bus and RAM bus
RAM 8 KB: 8 KB SRAM module
PCI selector: Module to connect between the USB host and PCI bus

<Microcontroller I/F> LSI CPU block

SYSRSTB: Reset signal for USB host and bus bridge
SIB: Signal for bus bridge serial data output and microcontroller serial data input
SOB: Signal for bus bridge serial data input and microcontroller serial data output
SCKB: Serial clock signal for bus bridge. Microcontroller is the master.
OPCIINT: USB-related interrupt output from the bus bridge
CFGSEL: Register/RAM access switching signal

・CKGEN

Clock generator with multiplication PLL using the 16.934 4 MHz clock as the source
Generates 27 MHz clock by dividing the clock obtained by multiplying 16.934 4 MHz with 8 by 5.

・USB buffer

DP and DM buffer used in USB communication

・48 MHz oscillation circuit

The block that oscillates 48 MHz clock for the USB clock

1.5.3 Flow for audio output from the USB device

When a USB device is connected to the USB connector, the LSI (host controller) recognizes the device.
The host controller load the compressed audio data from the USB device connected to the USB connector.
The loaded compressed audio data is stored in the RAM on Bus Bridge.
The stored compressed audio data is loaded on LSI CPU block by serial transfer.
The compressed audio data by serial reception from CSI is transferred to the Buffer Controller in LSI CD block via LSI CPU block.
The data is stored in the built-in 1 Mbit SRAM by RAMPNT and is transferred to Audio DSP by PLYPNT.
The compressed audio data is decoded for each audio data and output to DAC I/F as audio data.
The digital audio data input from DAC I/F into Audio DAC is output as analog audio data.

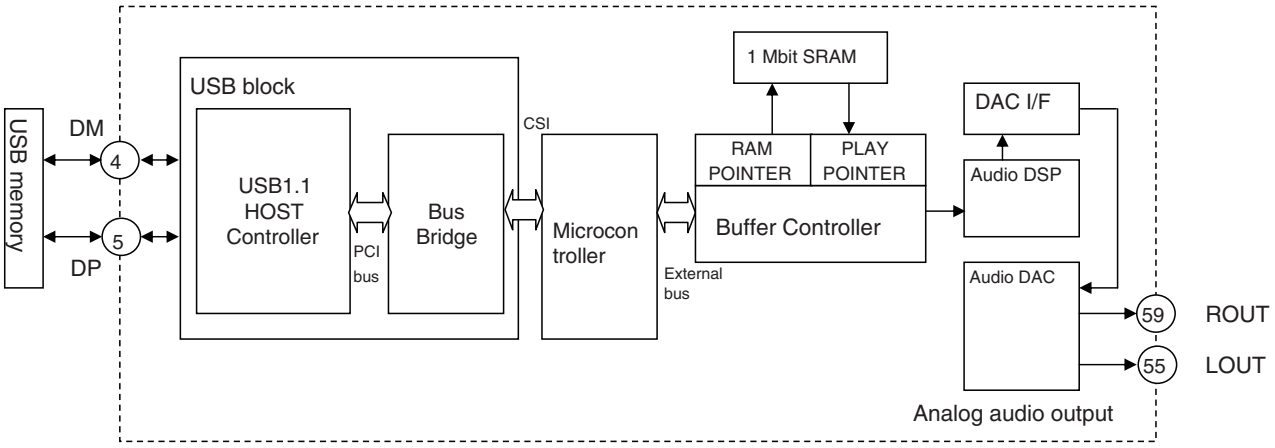


Fig.1.5.2 Flow for audio output from the USB device

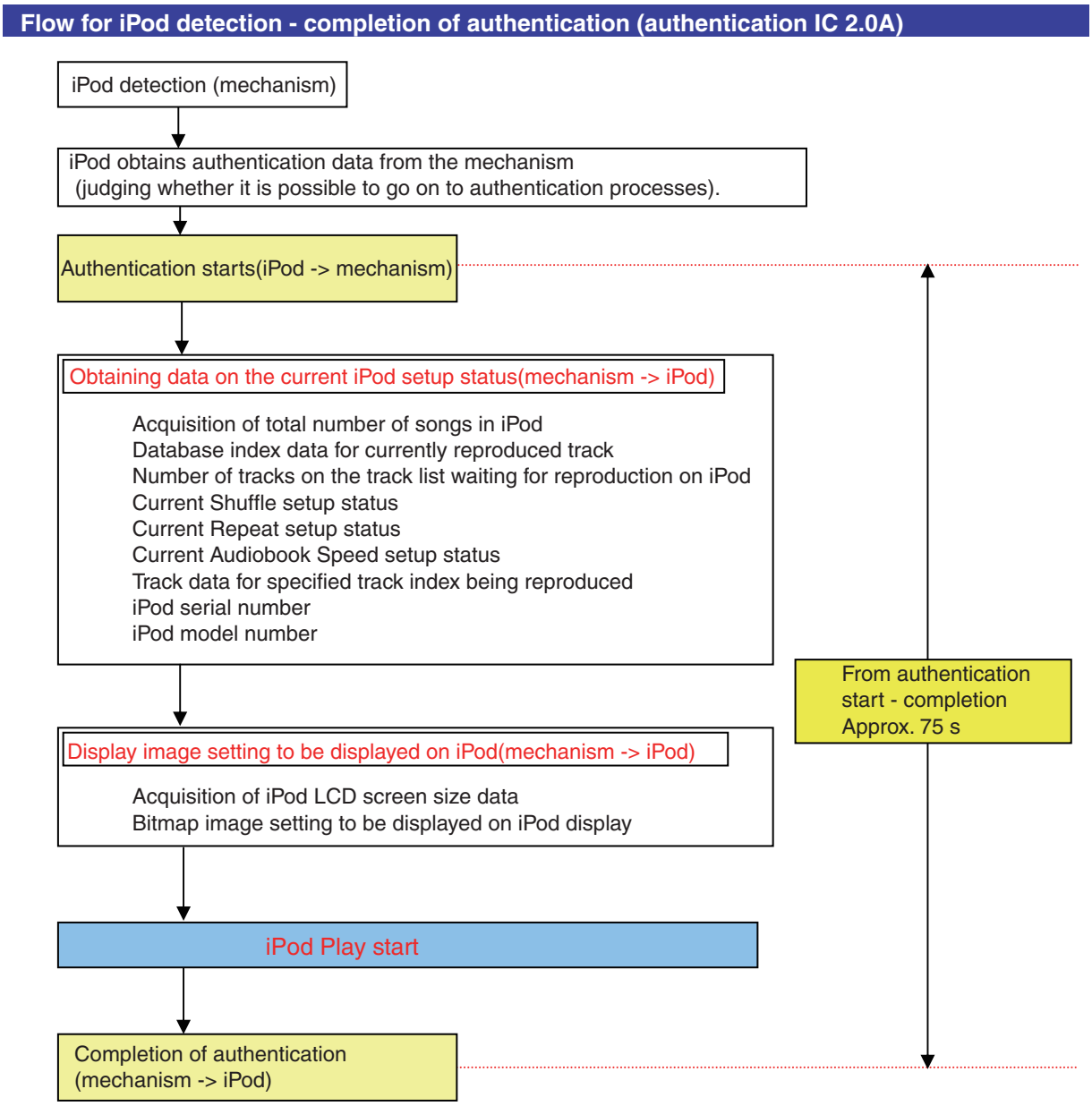
1.6 ABOUT iPod FUNCTIONS(iPod MODELS ONLY)

1.6.1 Outline

Unlike MSC devices, iPod executes all operations including PLAY/FF/REV and decoding of compressed file internally.
Digital audio data is transmitted to the mechanism through the USB block of LSI.
The mechanism will operate iPod by transmitting commands to iPod instead of file reproduction process and so forth.
Therefore the reproducible format and functions need to be compliant with iPod.
In addition, digital streaming may be impossible depending on the iPod generation and the firmware version.
These devices are handled as noncompliant devices and are not played.
iPod does not use the concept of folder configuration but access the category database.

1.6.2 iPod authentication flow

The flow from iPod detection to completion of authentication is shown as follows:

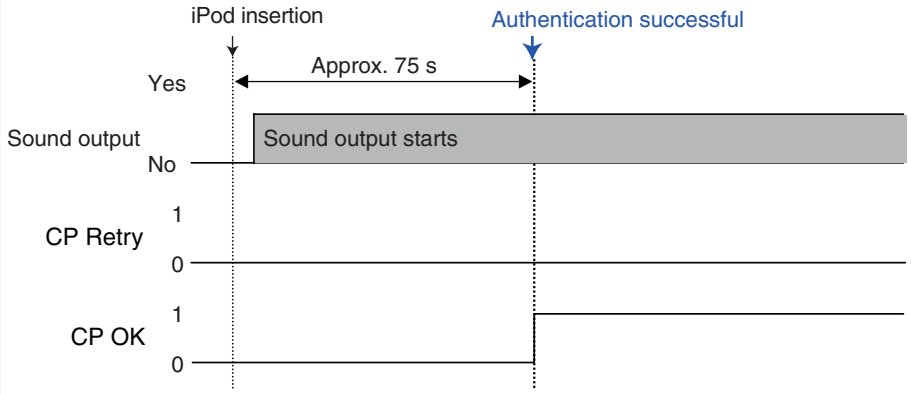


The status during iPod authentication is also provided as follows:

Authentication status when iPod is inserted

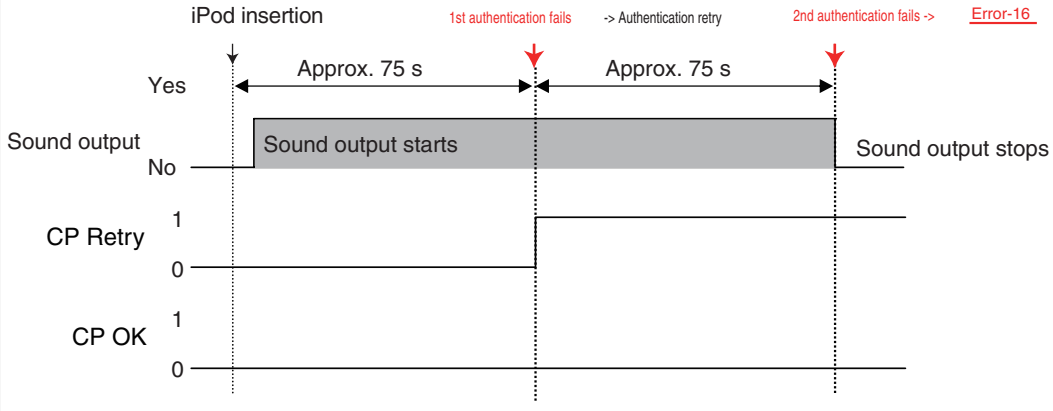
When iPod is inserted, authentication operation is executed between the CD mechanism (mounted with iPod authentication IC) and iPod.
Operation (status) by the CD mechanism and iPod in this case are shown as follows:

[When authentication is OK]
When authentication is successful in 1 try, sound output is continued (authentication OK).
When authentication fails in the 1st try and is successful in the 2nd try, sound output is continued (authentication OK).



* CP OK bit is set to "1" when authentication is successful.
* Since authentication is successful, CP Retry remains "0."

[When authentication is NG]
When authentication fails in the 1st try, the second authentication operation starts.
When authentication fails again in the 2nd try, ERR-16 (iPod authentication error) occurs and sound output is stopped (authentication NG).

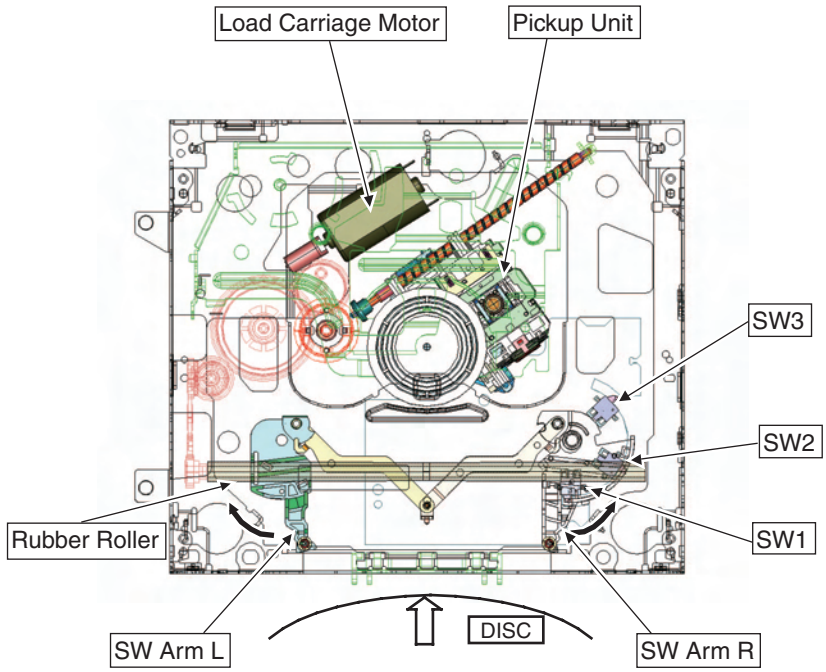


* When authentication retry starts, CP Retry bit is set to "1."
* Since authentication failed, CP Retry remains "0."
* Since authentication failed, Error-16 is generated and sound output is stopped.

2. MECHANISM DESCRIPTIONS

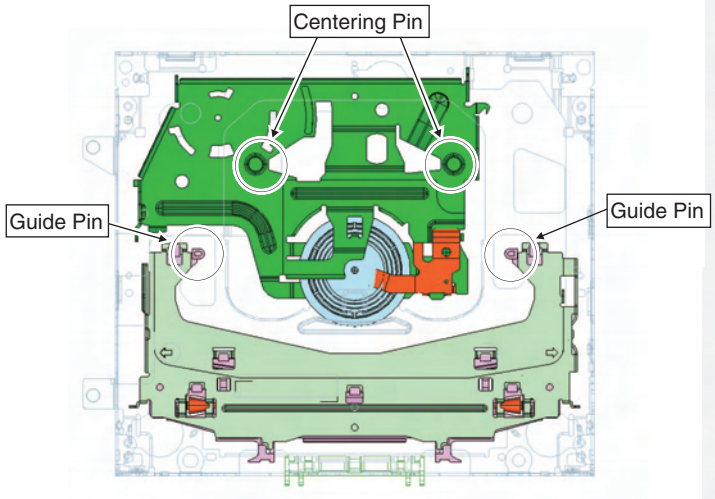
● Loading actions

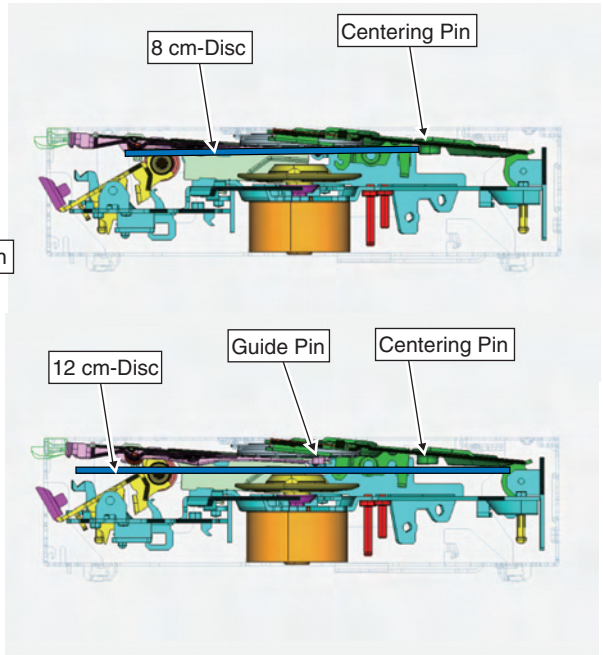
1. When a disc is inserted, SW Arm L and R rotate and SW1 is switched from ON to OFF.
   When SW1 is switched from ON to OFF, the Load Carriage Motor is started and the rubber roller rotates.
2. If the disc is a 12 cm-disc, SW3 is turned ON with SW Arm, and the microcomputer determines that the disc is a 12 cm-disc.
3. In case of an 8 cm-disc, SW3 is not turned ON, a clamp action is triggered, and the microcomputer determines that the disc is an 8 cm-disc.
   (The left and right of SW Arm are coupled, and when only one side is pushed, the coupled joint will lock, and the arms will not open more than a certain width (SW3 will not be turned ON).)



● Disc centering mechanism

1. 8 cm-disc is centered by the Guide Pins and the Centering Pins.
2. 12 cm-disc passes under the Guide Pins and the Centering Pins, and centered in the back position of the mechanism.





● Clamp actions mechanism

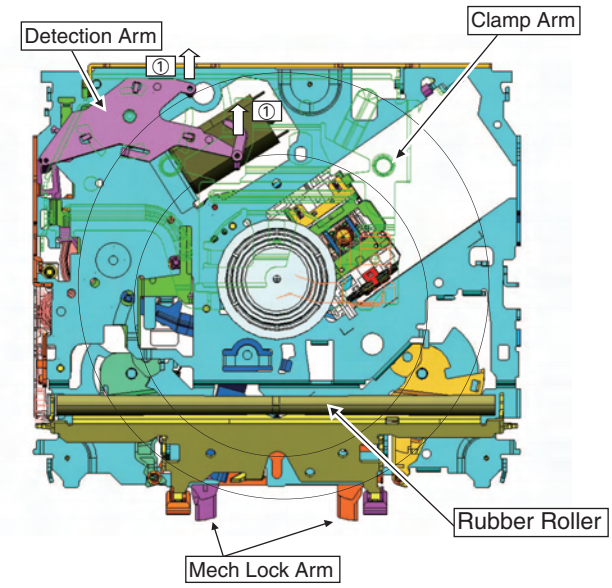
1. With an 8 or 12 cm-disc centered on the spindle, the Detection Arm is moved.
2. The movement of the Detection Arm engages the Loading Rack with the 2-Stage Gear.
3. The Clamp Lever slides and lowers the Clamp Arm (the disc is clamped).

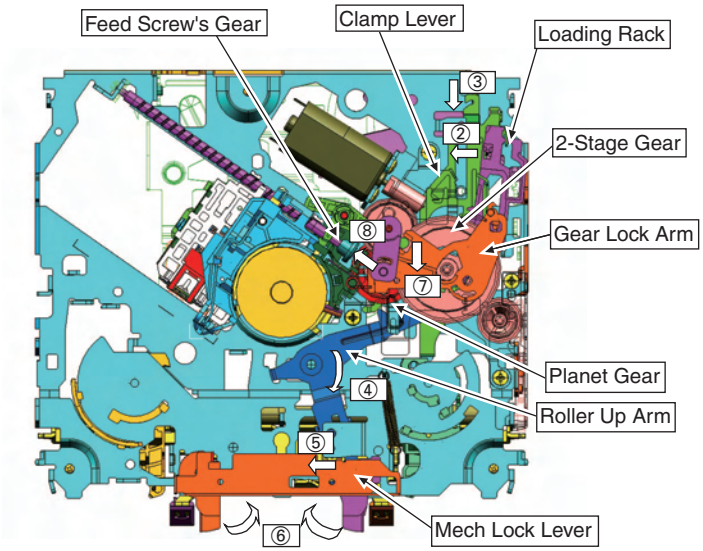
At the same time, the Roller Up Arm is rotated, and the Rubber Roller is separated from the disc.

Also the arm slides the Mechanical Lock Lever, turns the Mechanical Lock Arm, and releases the mechanical lock, completing the clamp operation.

4. When the clamp action is completed, the Clamp Lever rotates the Gear Lock Arm.

When the arm is rotated, the Planet Gear is separated from the 2-Stage Gear and engaged with the gear of the pickup feed screw, and the carriage operation will start





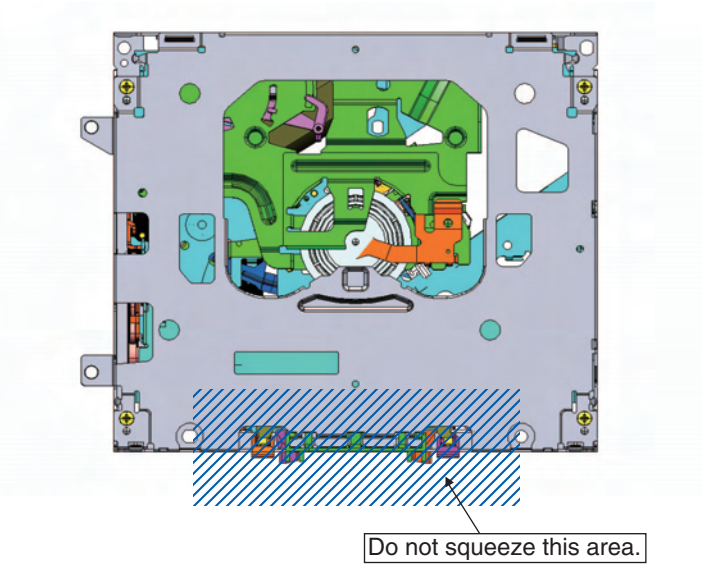
● Eject actions

1. When the Load Carriage Motor is rotated backward, and the pickup is fed to the inner periphery passing the home SW ON point, the eject action will start in the reverse order of the procedure mentioned earlier.
2. For a 12 cm-disc, Eject is completed when SW3 is switched OFF, ON, and OFF again.
3. For an 8 cm-disc, Eject is completed when SW2 is switched OFF, ON, and OFF again.

3. DISASSEMBLY

● How to hold the Mechanism Unit

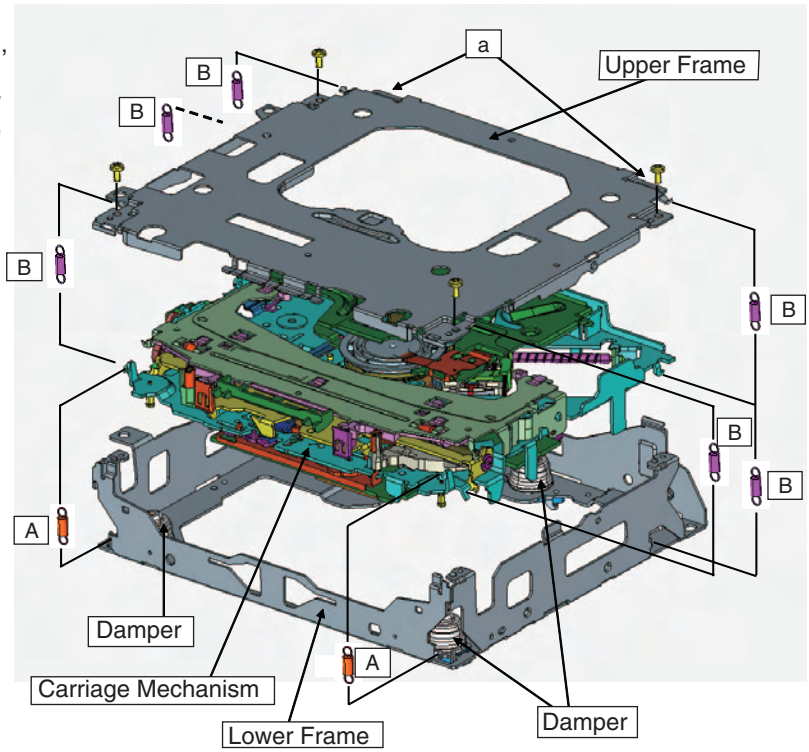
1. Hold the Upper and Lower Frames.
2. Do not hold the front portion of the Upper Frame, because it is not very solid.



● Removing the Upper and Lower Frames

1. With a disc inserted and clamped in the mechanism, remove the two Springs (A), the six Springs (B), and the four Screws.
2. Turn the Upper Frame using the part "a" as a pivot, and remove the Upper Frame.
3. While lifting the Carriage Mechanism, remove it from the three Dampers.

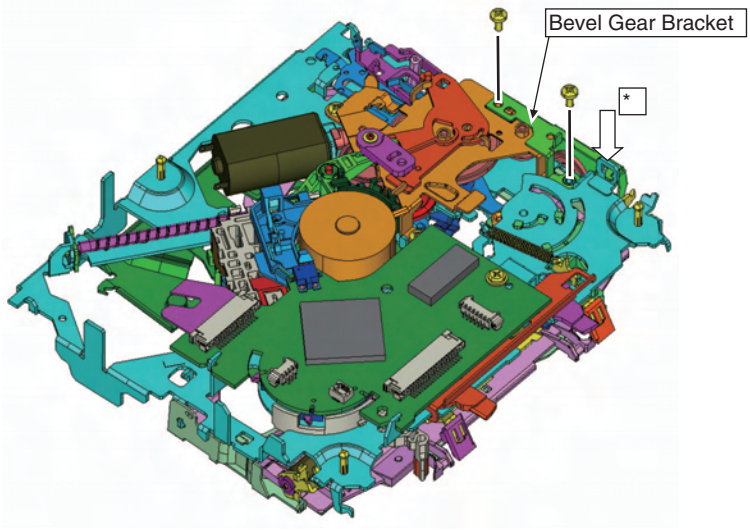
Caution: When assembling, be sure to apply some alcohol to the Dampers and assemble the mechanism in a clamped state.

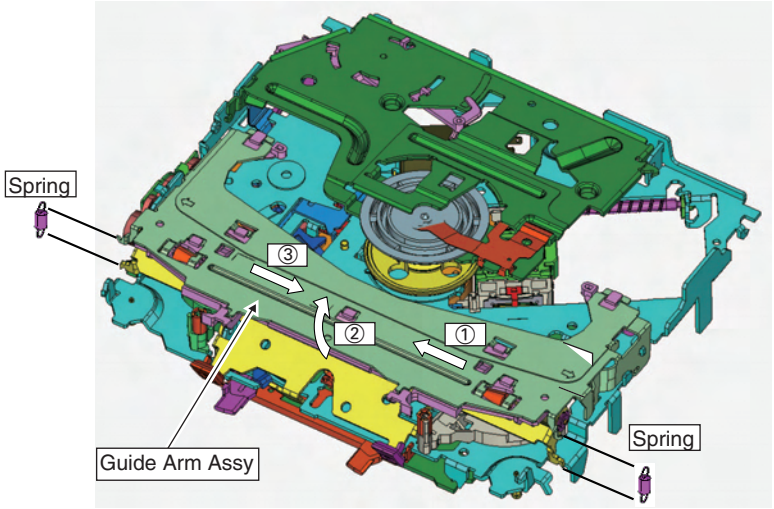


● Removing the Guide Arm Assy

1. Remove the Upper and Lower Frames and set the mechanism to the eject mode.
2. Remove the two Screws and Bevel Gear Bracket. (Note that the gears will come off.)
3. Remove the two Springs from the left and right sides.
4. Slide the Guide Arm Assy to the left, and turn it upward.
5. When it is turned about 45 degrees, slide it to the right and remove.

Caution: When assembling, assemble with the Bevel Gear Bracket moved to the direction of the arrow (*).

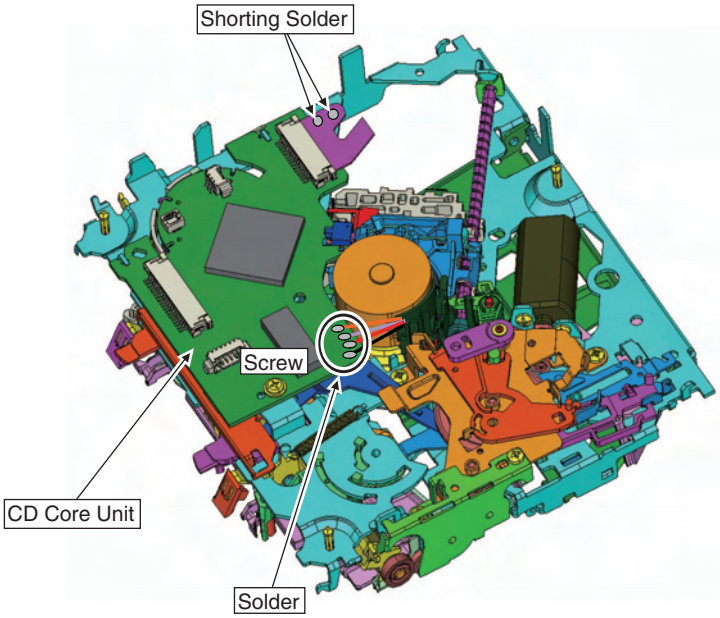




● How to remove the CD Core Unit

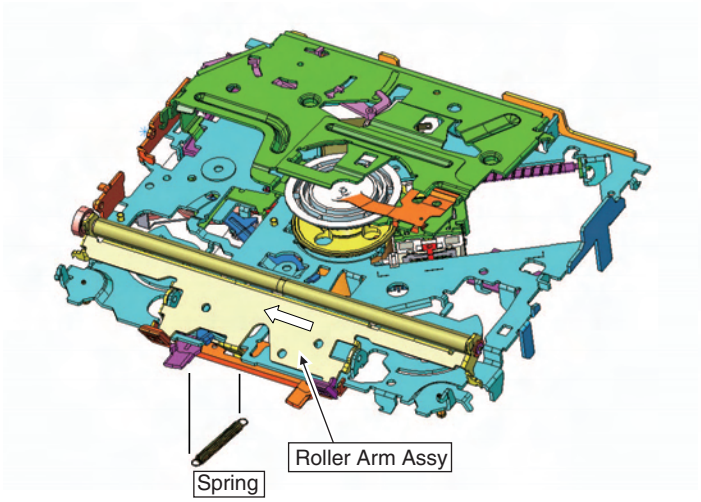
1. Apply Shorting Solder to the flexible cable of the Pickup, and disconnect it from the connector.
2. Unsolder the four leads, and loosen the Screw.
3. Remove the CD Core Unit.

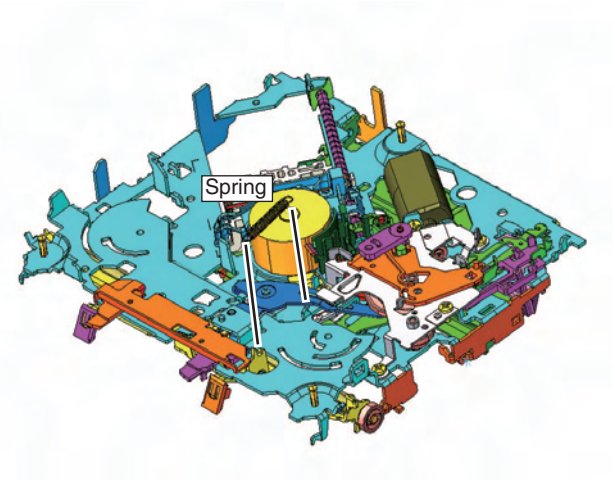
Caution: When assembling the CD Core Unit, assemble it with the SW in a clamped state so as not to damage it.



● How to remove the Roller Arm Assy

1. Remove the Guide Arm Assy.
2. Remove the CD Core Unit. (If the Spring can be removed, the unit need not be removed, depending on the type of CD Core Unit.)
3. Remove the Spring.
4. Slide the Roller Arm Assy to the left.



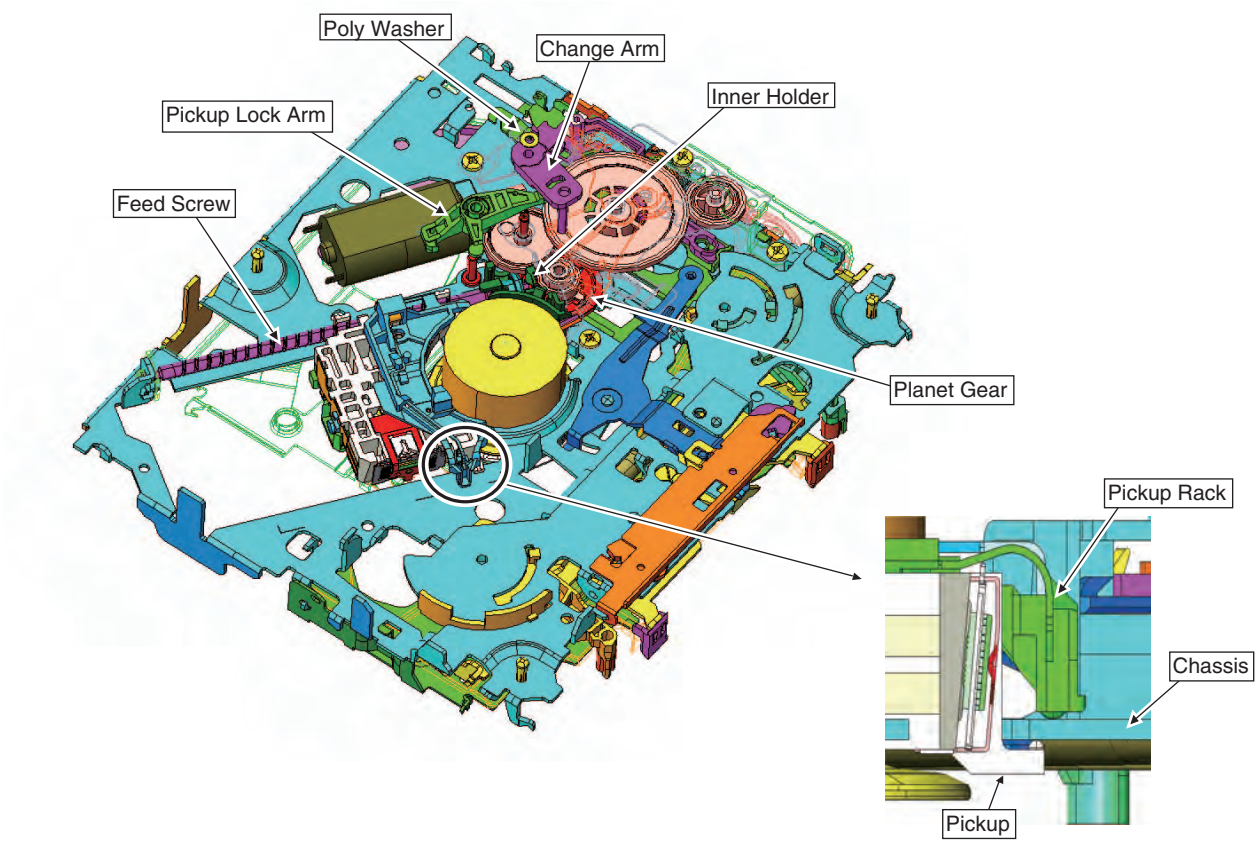


● How to remove the Pickup Unit

1. Make the system in the carriage mechanism mode, and have it clamped.
2. Remove the CD Core Unit and remove the leads from the Inner Holder.
3. Remove the Poly Washer, Change Arm, and Pickup Lock Arm.
4. While releasing from the hook of the Inner Holder, lift the end of the Feed Screw.

Caution: When assembling, move the Planet Gear to the load/eject position before setting the Feed Screw in the Inner Holder.

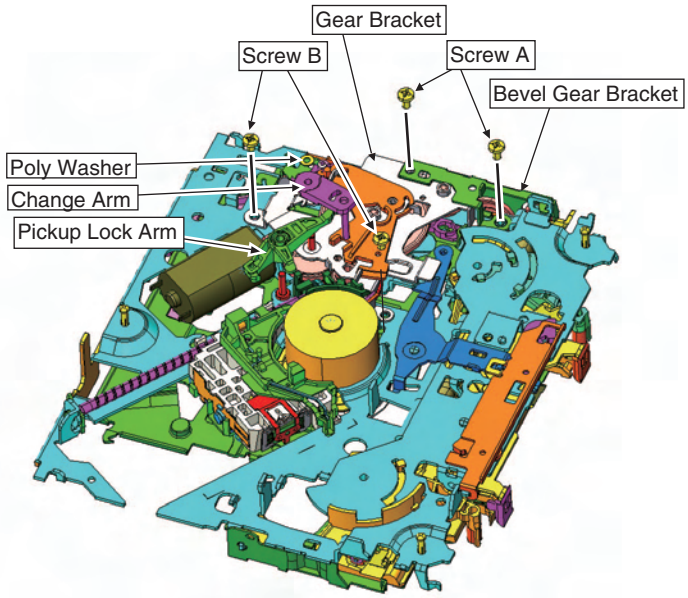
Assemble the sub unit side of the Pickup, taking the plate (Chassis) in-between. When treating the leads of the Load Carriage Motor Assy, do not make them loose over the Feed Screw.

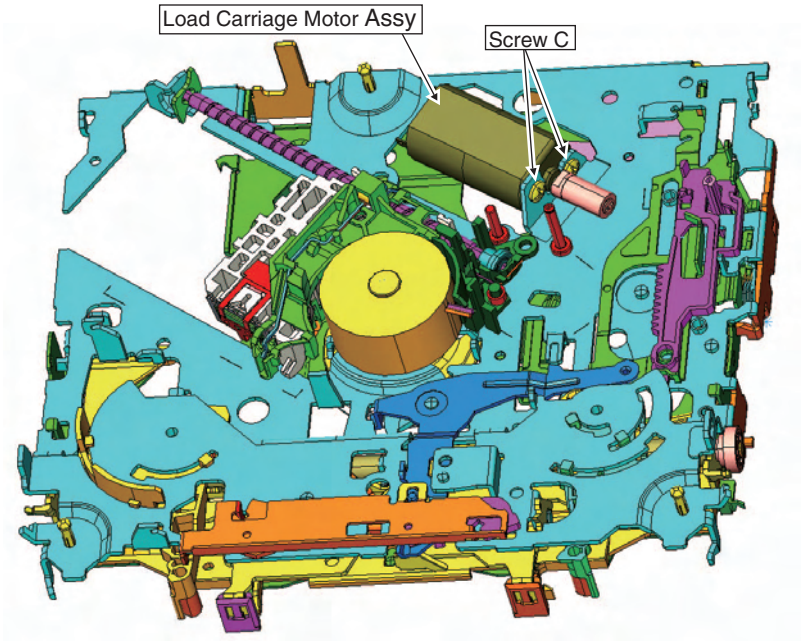


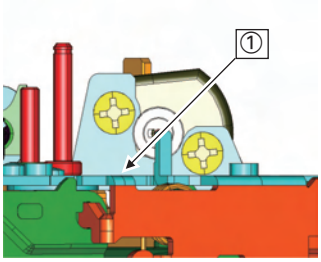
● How to remove the Load Carriage Motor Assy

1. Make the system in the carriage mechanism mode, and have it clamped.
2. Release the leads (orange and purple) of Load Carriage Motor Assy from the CD Core Unit and remove the holder.
3. Remove the Poly Washer, Change Arm, and Pickup Lock Arm.
4. Remove the two Screws (A) and the Bevel Gear Bracket (Note that the gears will come off).
5. Remove the two Screws (B) and the Gear Bracket (remove the CD Core Unit, if necessary), and remove all the gears.
6. Remove the two Screws (C) and the Load Carriage Motor Assy.

Caution: When assembling the Load Carriage Motor Assy, move it to the direction shown in the illustration (①).
When treating the leads of the Load Carriage Motor Assy, do not make them loose over the Feed Screw.



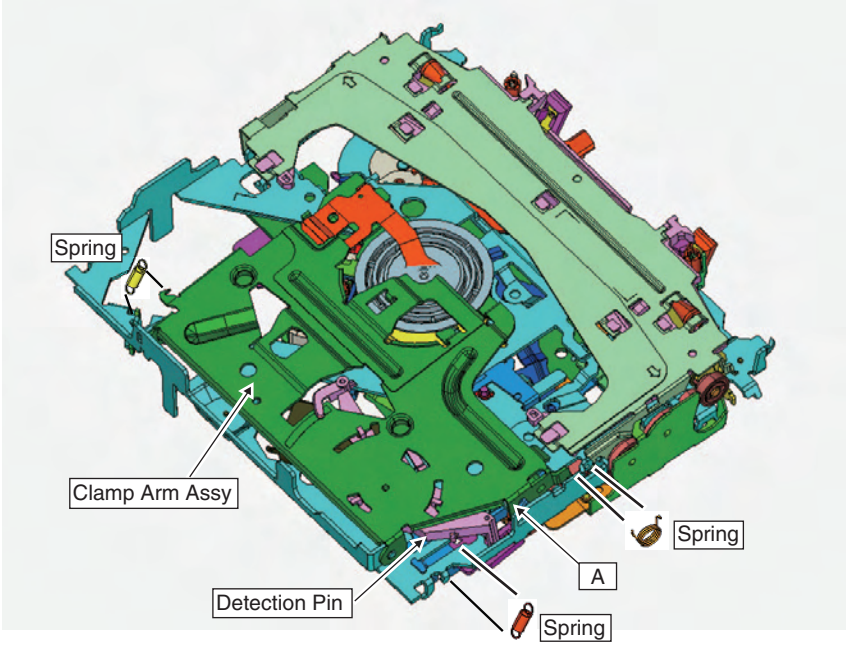


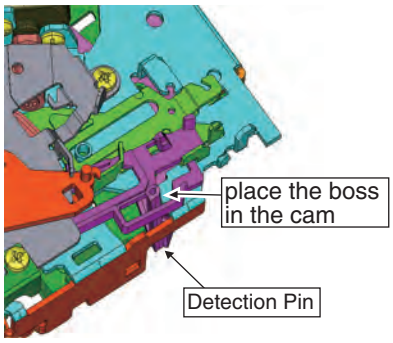


● How to remove the Clamp Arm Assy

1. Make the system in the carriage mechanism mode, and set the mechanism to the eject mode.
2. Remove the three Springs.
3. While pressing the position A, turn the Clamp Arm Assy upward, slide it to the left, and remove.

Caution: When assembling, place the boss of the Detection Pin in the cam unit of the Loading Rack.





● How to remove the Spindle Motor Assy

1.Make the system in the carriage mechanism mode, and have it clamped.
2.Remove the CD Core Unit and remove the leads from the Inner Holder.
3.Set the mechanism to the eject mode and remove the Clamp Arm Assy.
4.Set the mechanism to the clamped and move the Pickup to circumference.
5.Remove the two Screws, and remove the Spindle Motor Assy.